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~~On page 12, paragraph beginning at line 14, amend as follows:~~

IDC-A4,AMD

Referring now to Figs. 2A and 2B, a shoot-through current suppression circuit 200 is shown as an example of the boundary circuit. Fig. 2A is a logic circuit diagram showing the circuit configuration of the shoot-through current suppression circuit 200. Fig. 2B shows a truth table for the shoot-through current suppression circuit 200. Use of the shoot-through current suppression circuit 200 can suppress the transmission of an indeterminate signal from a circuit area where power supply is OFF to a circuit area where power supply is ON. The use of this circuit can substantially prevent the indeterminate signal. This allows suppressing or preventing a shoot~~short~~-through current to occur in the next-stage circuit to reduce the power consumption of the entire chip.

~~On page 13, paragraph beginning at line 7, amend as follows:~~

IDC-A5,AMD,M

The operation of the shoot~~short~~-through current suppression circuit 200 will be explained with reference to Figs. 2A and 2B. Fig. 2B shows the relationship of an input signal "input" to the input terminal 201, an enable signal "enable" to the enable terminal 204, and an output signal "output" from the output terminal 205. The symbol "X" in the table indicates that a signal is indeterminate, "0" indicates that the output voltage is Low, and "1" indicates that the output voltage is High. If the first circuit area 101 is OFF, an indeterminate signal is input to the input terminal 201.

~~On page 13, paragraph beginning at line 17, amend as follows:~~

Specifically, if the first circuit area 101 is OFF, the output signal from the first circuit area 101 to the second circuit area 102 is indeterminate between High and Low. Thus, a signal with an intermediate voltage level is input to the second circuit area 102. This causes the shoot~~short~~-through current to occur in the second circuit area 102. To prevent this, this

embodiment controls the operation in such a way that the enable signal input to the NAND gate 203 is "0", which is "Low", when the first circuit area 101 is OFF.

~~On page 14, paragraph beginning at line 2, amend as follows:~~

By setting the enable signal to "0", it is able to determine and keep the output signal from the output terminal 205 to be "1", that is, the output voltage to be "High". As described above, if the circuit is OFF, its output is indeterminate between High and Low, and thus a signal with an intermediate voltage level between High and Low is input to the receiving circuit. The circuit configuration in this embodiment, however, can suppress the shoot~~short~~-through current in the ON-state circuit area due to the indeterminate signal from the OFF-state circuit area.

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B ~~On page 12~~ 14, ~~paragraph beginning at line 12, amend as follows:~~

If the first circuit area is ON, the shoot~~short~~-through current suppression circuit 200 is controlled in such a way that the enable signal is "1". Thereby, if the input signal from the internal circuit of the first circuit area 101 to the input terminal 201 is "0", the output signal from the output terminal 205 to the internal circuit of the second circuit area 102 is determined to be "0", and if the input signal is "1", the output signal is "1". If the input signal is indeterminate and the enable signal is "1" or indeterminate, the output signal is indeterminate.

~~On page 18, paragraph beginning at line 21, amend as follows:~~

IDC-A6,AMD,M

Though several examples of the boundary circuit are shown above, the boundary circuit to which the present invention is applicable is not limited thereto. The above circuits may be inserted between the circuit areas driven by different power systems separately or in combination with others. For example, it is possible to insert the level conversion circuit or